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Design of 16-Bit Low Power Carry Select Adder using D-Flip Flop

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***Abstract*—Circuit like adders are the basic component for any of the processors like digital signal processors. An area and lower consumption efficient adder design are necessary for the high speed applications. In many operation, carry propogation through the adder is a critical section. Carry select adder (CSA) is efficient for the low power applications, produces the partial sum and carry by generating independently multiple carries. Hence, there is a chance in the CSA to reducing the power and area consumption. Conventional CSA uses the two pair of ripple carry adder (RCA) with cin =1 and cin =0 hence consumes more power. Complimentary pass transistor based CSA designed using inverter at the input side to drive the gate of MOS transistors and to strengthen the signal at the output side therefore it's not an area efficient. The proposed adder uses the true single phase clock (TSPC) D-Flip flop instead of using RCA and BEC in the conventional method. This saves a significant power and area with reduced number of transistors. The 16-bit adder design is implemented in semi custom 180-nm technologies which save 75% and 25% of the power over the conventional adder and normal TSPC based adder respectively. The proposed adder is good for the power delay product which reduced to 75% and 50% over the conventional based RCA and normal TSPC adder respectively.**

***Index Terms*— CS adder, modified TSPC, D-flip flop, low power, power delay product.**

I. INTRODUCTION

Speed is an important parameter for the DSP applications, to increase the speed, circuit should have minimum delay [1].In order to have high performance processors for the signal processing applications, an efficient low power addition is needed. In processor like Pentium and arm, number of instructions will be executed in a single cycle.

Adders with high performance in the final stage of a multiplier plays Important role in the performance of overall circuits. The addition speed is limited by the propagation of carry signal in adders. Carry select adder delay is in between ripple carry adder and area of the carry look ahead adders circuits. CSA reduces the cost and improves the performances. There are two blocks in carry select adder: for the first one assuming cin=0, for other one cin=1. Hence it avoids propagation of carries over the block by selecting independently generated multiple local carries. The results generate two pre- computed carry and sum output. The output at final is selected based on the original carry signal given to multiplexer. CSA classified as: Square-root CSA which is obtained by equalizing delay via two carry chains and the signal of the previous

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stage of the multiplexer. This is in binary weighted form also called a non-linear CSA. In the proposed design, a technique is introduced that results in low power called as d-flip-flop with true single phase clock which increase the speed and minimizes power drastically of the carry select adder. The proposed design greatly minimizes the delay introduced by Binary to excess-1 converter used in conventional CSA to some level. The main advantage of the d-flip flop comes from high speed than the n- bit full adder structure used in conventional adder.

II. Related Work

A. 16-bit Carry Select Adder using RCA

Ripple carry adder is implemented cascading one bit full adder block and produces the sum and carry signal. The sum of succeeding block is produced sequentially only after the preceding block is summed and carry propagated to the next. This design is efficient in terms of area and simple but delay in the propagation of the carry signal from preceding block to next hence slower in speed. In CSA, stages of n-bit divided into m blocks. Each m blocks consists of two RCA's with each having cin=0 and cin=1 respectively. At the end, the final sum is obtained through the multiplexer according to the original cin is given to the MUX [3] [4]. Square root CSA with 16-bit is as shown in Fig. 1. CSLA performs operation very faster because it will not wait for carry from the preceding block instead of that computes sum with independent given carry signal. Hence can get actual result in MUX output with little amount of delay of each one bit full adder.

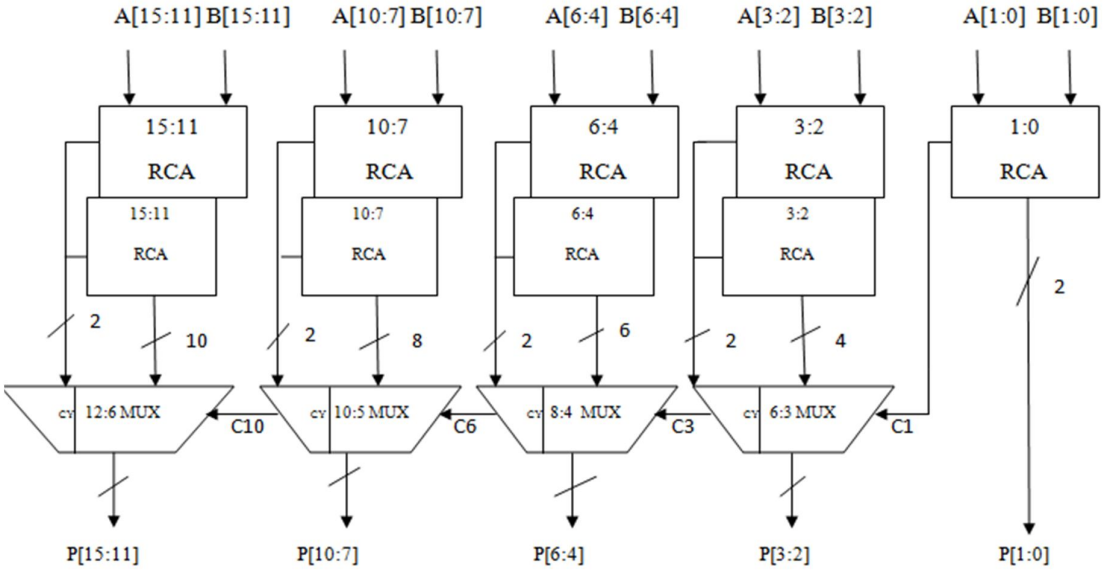

Fig. 1 16-bit Square root CSLA using RCA

B. 16-bit Carry Select Adder using Binary to Excess-1 Converter

To minimize the power and area of regular carry select adder, binary to excess-1 converter is introduced with replacement of cin=1. BEC provides an extraordinary performance over the regular CSA. To get efficient low power carry select adder, binary to excess-1 converter is used with ripple carry adder along with multiplexer for getting fast addition for un even arrival of the input signal with different time. Input to multiplexer is one from RCA block with cin=0 and another one is from binary to excess-1 converter [4]. The 16-bit Square-Root CSLA with BEC is shown in Fig.2.

C. 16-bit Carry select adder with normal D-flip flop with normal True single phase clock.

True single phase clock is one which takes true phase of the clock and it will not take complements of the clock. Flip flops are used to store single bit of data. While considering the regular CSLA and CSLA with binary to excess -one converter the carry select adder using flip flops are more efficient than those [5]. Flip flops becoming more popular in designing an adder circuits. A dual clock pulse generator required to produce

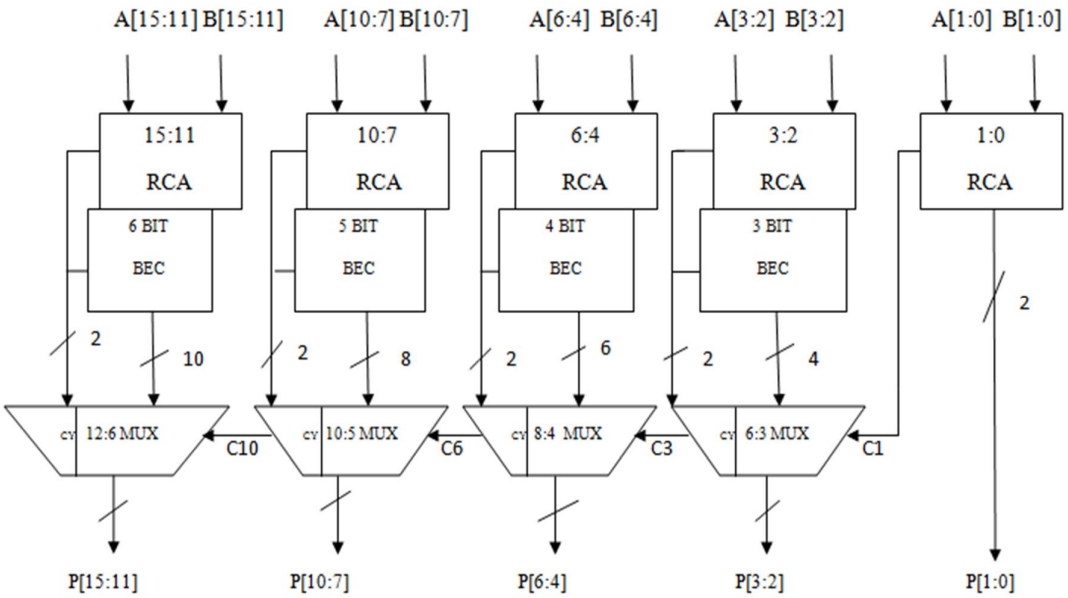

Fig. 2 16 Bit Square-Root CSLA with BEC

pulses in both side of the clock edges i.e. raising edge and falling edge of the clock and also the same pulse can be used to switch the ground. Here, the input D is given to the both NMOS and PMOS and implemented using transistor switching logic.

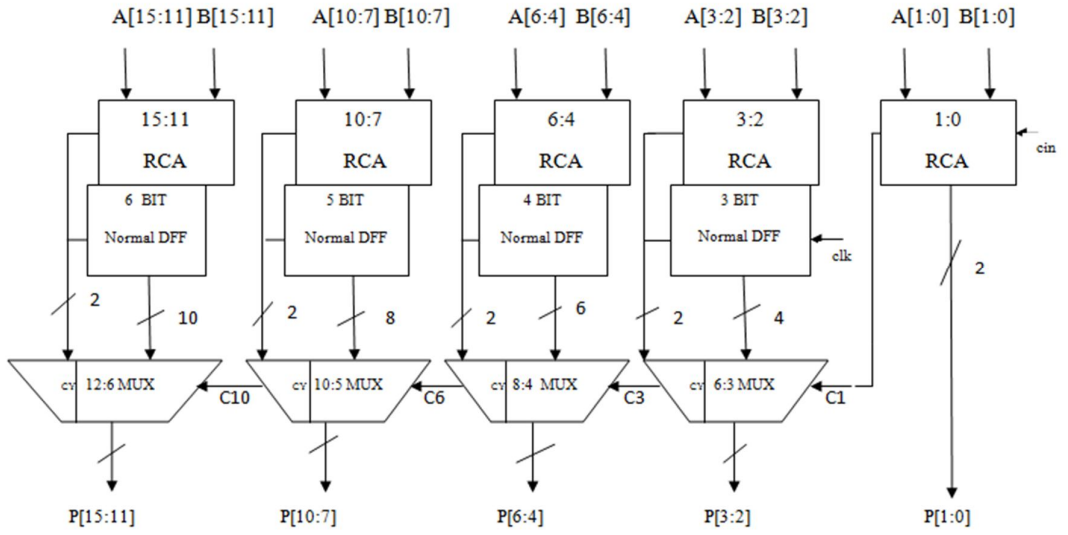

Fig. 3 16- Bit Square-Root CSLA using Normal D-flip flop

This design uses transistors with less number i.e. 11 therefore power consumed will be less compared to other circuits. But only the disadvantages are when there is complexity in cascading units such as multipliers. Here, The 16- bit adder with carry select using normal D-flip flop uses the regular block of RCA for addition with cin, when clock becomes zero the adder circuit performs the addition and stores the result in flip flops. When clock becomes high adder performs operation and gives to multiplexer. The stored data in flip flop will

be latches when clock becomes high. So that actual sum and carry is produced during one complete clock cycle. The 16- bit CSA using Normal D-flip flop as Shown below Fig. 3.

III. MODIFIED TSPC

A. Normal TSPC

True single phase clock has a single clock and it's never be inverted. Clock given to NMOS and PMOS devices. Output is constantly affected by changes in the inputs with variation in the clock. True single phase clock which reduces the overal power required for operation of the circuit. It requires less transistor therefore consumes less power. TSPC will acts as master and slave circuits [6]. Fig. 4. Shows normal true single phase clock flip flop.

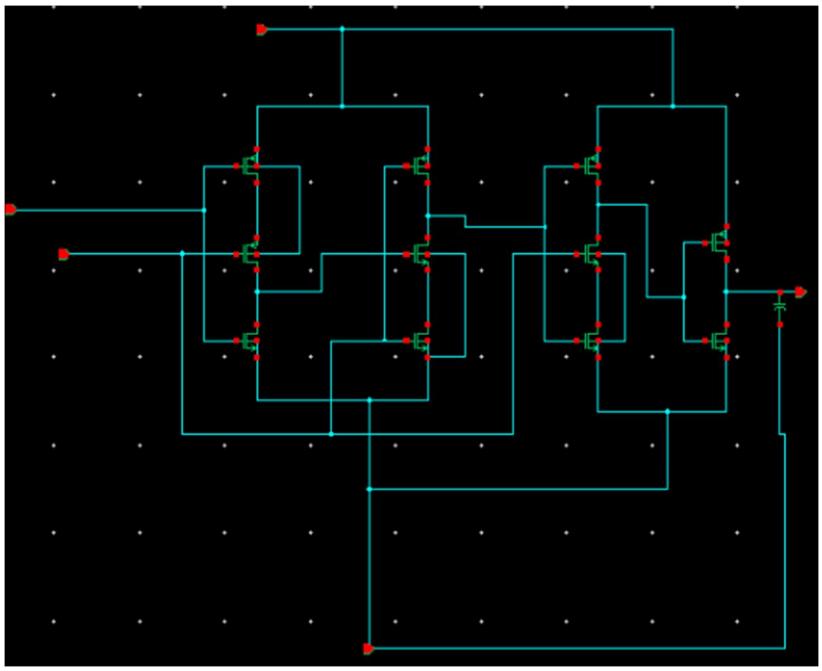

Fig. 4 Normal true single phase clock

B. Modified TSPC

A transistor which is clocked by a single clock pulse is known as True single phase clock because it is triggered by the clock with rising edge. It works with according to clock, flip flop transitions occurs with clock on the rising edge. When D is low and clock is at low, PMOS will be turned ON which connects the VDD to output hence logic '1' is the output at node near the PMOS transistor. Due to that logic state '1' the NMOS will be turned ON discharging path will takes place hence logic '0'. The logic '0' is stored at a node say A node in the master block and in the slave, whatever the logic state at a node say node A i.e. '0'. Due to this logic '0' the PMOS will be turned ON in slave block hence logic '1' at PMOS drain terminal which is given to gate terminal of the NMOS transistor of the inverter block hence will get the output same as in the input D. Inverted clock with inverter circuit is eliminated so that greatly reduced in the delay and power. Modified TSPC is as shown in Fig. 5.

IV. PROPOSED ARCHITECTURE

A. Carry Select Adder using D-Flip Flop with Modified True Single Phase Clock.

Here, we are using positive edge D- flip flop with Modified TSPC to results sum and carry output. It reduces the power consumed compared to Normal TSPC because usage of the transistor in the Modified TSPC will

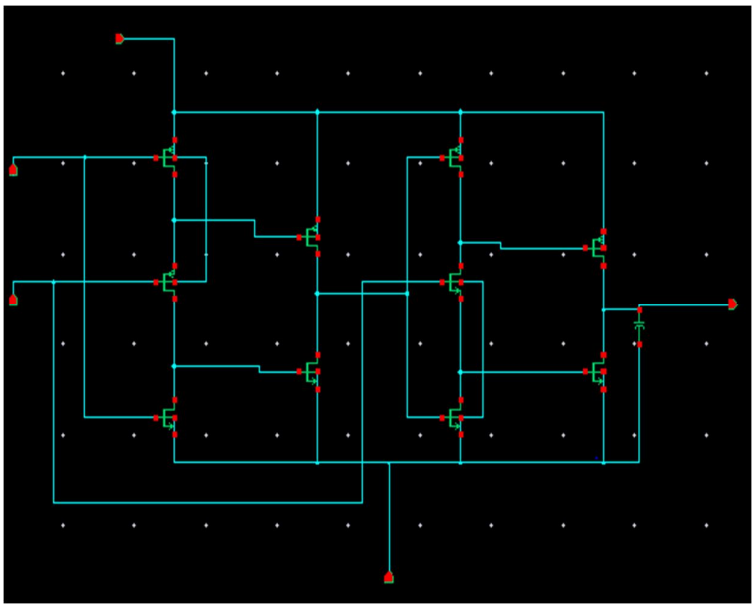

Fig. 5 Modified true single phase clock flip flop

be less [6]. It consists of regular CSA, D-flip flop which replaces the BEC and RCA blocks in the regular CSLA design, Multiplexer in the last stage to select the actual sum and carry depending upon the actual clock signal.

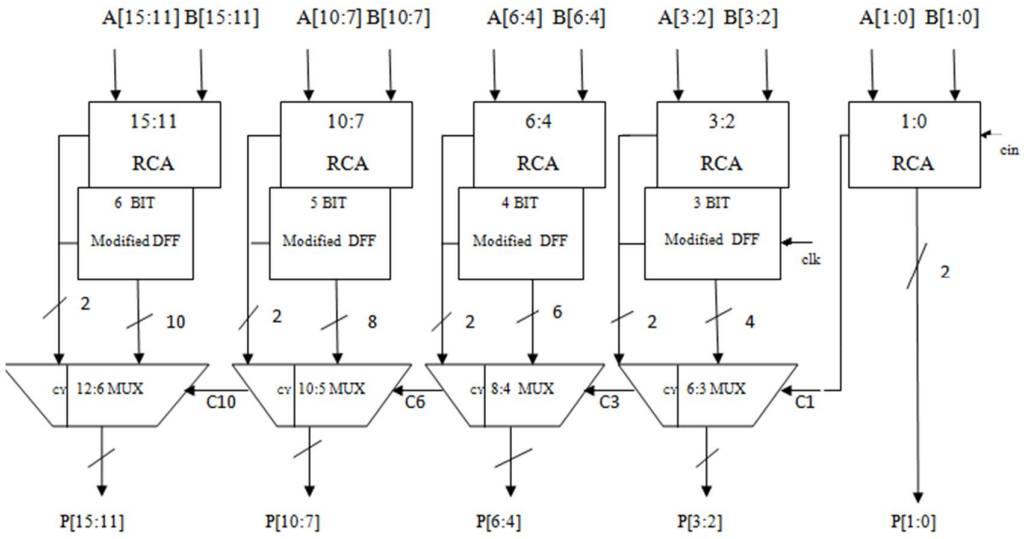

Fig. 6 16-bit CSLA using modified D- Flip flop

When clk becomes low adder circuit performs the operation and holds the result in D-flip flop and when clk becomes high it performs the operation and gives to multiplexer. The final result will be obtained by multiplexer in one complete clock cycle. That is if multiplexer control signal is zero, then we will get the output to next succeeding with cin=0. If it is one, we will get the output with cin=1.Carry is propagated from previous block multiplexer block multiplexer. With the use of D-flip flop operation speed will be increased and uses less amount of power. 16-bit CSLA using Modified D- Flip flop is given in Fig. 6.

V. Comparison of Proposed CSLA with Other adders and simulation results

The carry select adder with 16-bit using D-flip flop is implemented and simulated in cadence 180-nm virtuoso editing tool. The proposed architecture compared with other existing architecture. The overall power consumption is reduced with less delay and the product of power delay is totally reduced with other regular adders hence proposed design is best suited for arithmetic applications as well as DSP Applications. Table 1 Shows the Comparison of 16- bit Proposed CSLA with Regular adders respectively. Here the half of the power will be reduced from the proposed method when compared with the carry select adder using normal D-flip flop. And also transistor number count is reduced from the regular CSLA adder circuits. Simulated in 100MHZ activity and the clock pulse and width will be 10ns and 5ns respectively. The 16- bit input and output waveform is given in Fig. 7 and Fig. 8 respectively.

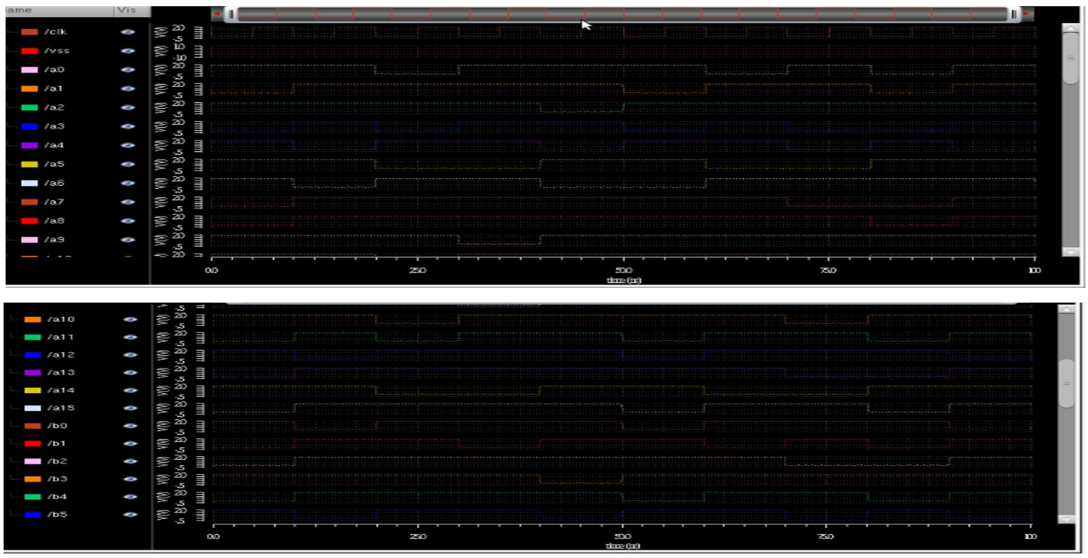

Fig. 7 16-bit proposed CS adder input waveforms

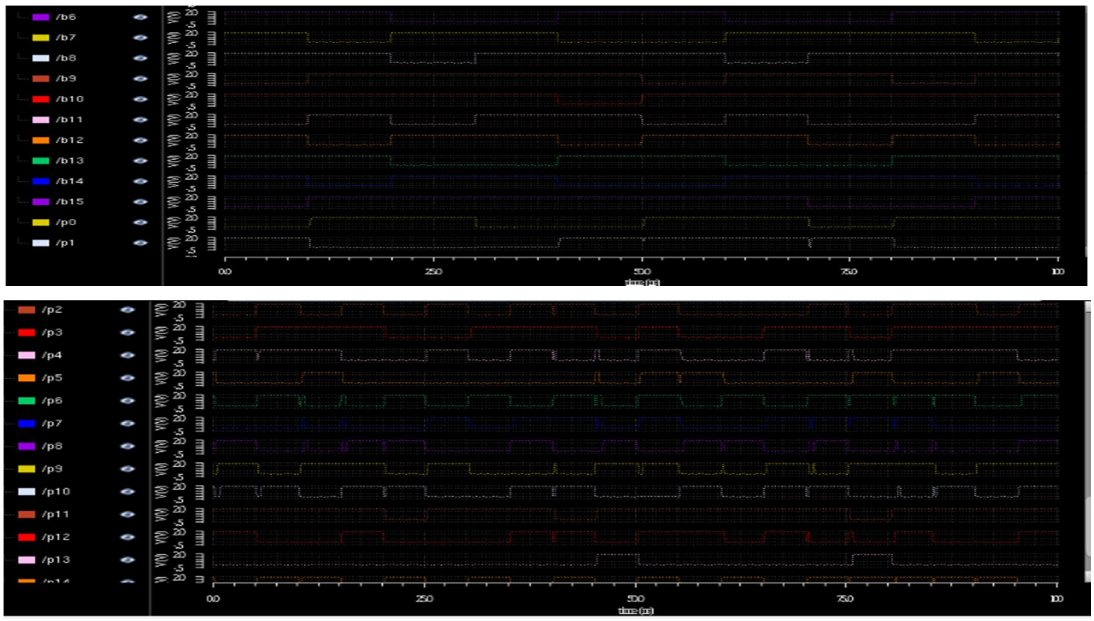

Fig. 8 Output waveforms of 16-bit proposed Carry Select adder

TABLE I: 16-BIT CARRY SELECT ADDER COMPARISON RESULT

Adders	Power Consumption (mw)	Delay (ns)	Power Delay Product ($x10^{12}$)
Carry select adder using dual RCA	1.106	59.71	66.03
Carry select adder using RCA and BEC	1.161	59.71	69.32
CS adder using RCA and Normal DFF	0.019	59.69	11.34
Proposed CSA using RCA and Modified D-flip flop	0.011	59.69	0.656

VI. CONCLUSION

In VLSI Design Technology, The power consumption, delay and area are the main factors to determine the overall performance of the circuit. The regular adder circuits consume more power compared to proposed design. A well organized CS adder uses the power supply of 1.8V and designed in 180-nm technology. The proposed 16-bit carry select adder using D-flip flop with Modified TSPC is consumes less power with improved performance. Hence the proposed adder design is best suited for arithmetic and DSP applications compared to other topologies. Obtained better power delay product and reduced in power consumption. In the future, designing a Carry select adder with new improvements in the flip flops circuit in such a way that, the adder circuit should consume less delay. The projected plan can also extend for 32-Bit, 64-bit and 128-bit also which gives better performance over the power utilization and figure of merits.

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